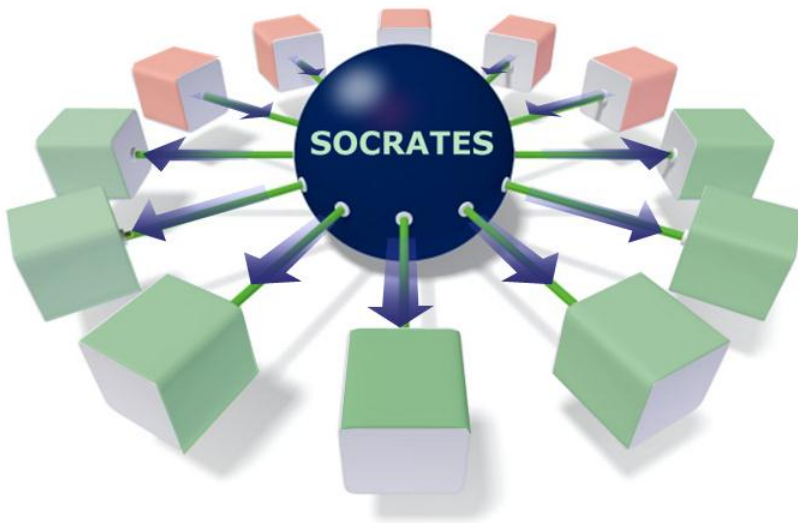


### IP Integration and Chip Assembly



### STANDARDIZE, CENTRALIZE, SYNCHRONIZE

**Socrates Weaver** manages the complete assembly of a complex system from IP to top level, enabling design/integration engineers to deliver rapid and robust integration views throughout the design process.

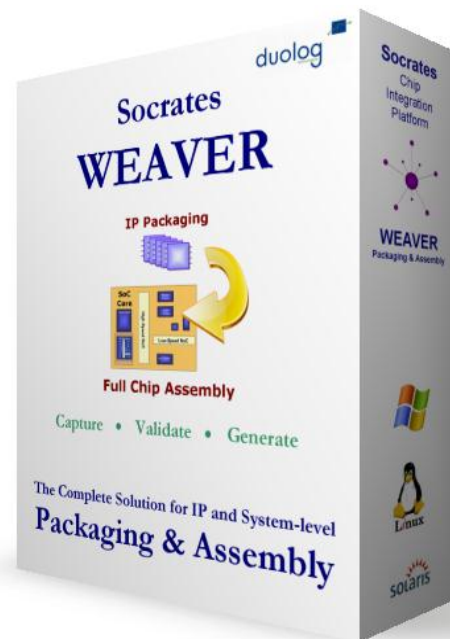
Weaver provides a complete IP packaging and standardization flow, creating formalized views of IP design data. This facilitates increased IP reuse and promotes a more formal method of integration.

IP is rapidly integrated using Weaver's highly efficient rules-based integration methodology. This unique methodology delivers levels of productivity an order of magnitude higher than conventional flows.

Efficient, effective and robust chip integration is an essential element of any successful SoC development.

Time-to-market and cost pressures are dictating ever higher levels of IP use and reuse. Engineering teams are growing in size and diversity, with software playing an increasingly prominent role. These teams require simultaneous access to different views of the same design data throughout the lifetime of the project. It is vital that all teams access their information from a single source to avoid catastrophic data duplication, misinterpretation or misalignment errors.

The **Socrates Chip Integration Platform** acts as a hub for chip integration, standardizing IP and system metadata, centralizing design information and synchronizing design teams by auto-generating multiple views from a single, verified source.



***On first-time usage, Weaver gives an immediate integration productivity gain of 4x-8. Thereafter, Weaver can deliver up to 50x more productivity than conventional integration flows.***

## FEATURES

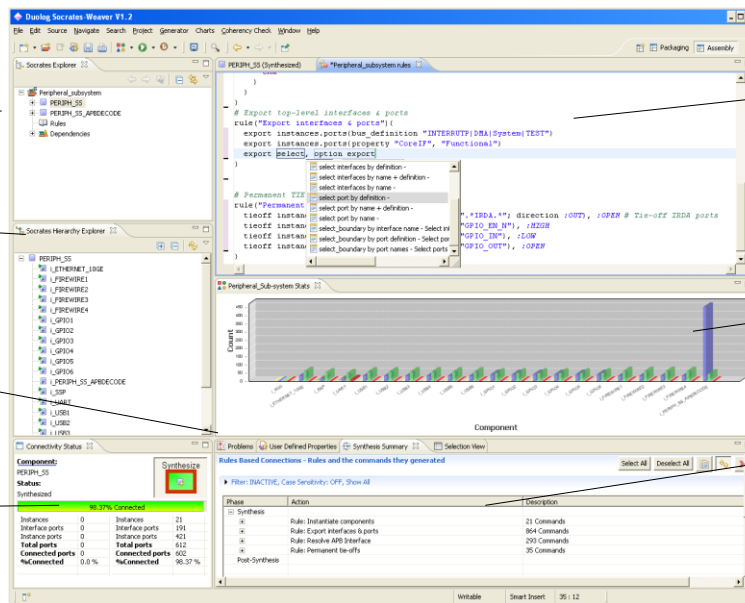
- A complete IP standardization flow, including the ability to import HDL/IP-XACT interface descriptions and capture additional data and properties
- Rapid IP integration/system assembly using either manual or rules-based workflows
- IP instantiation, configuration and connectivity
- Highly productive and robust connectivity mechanisms
- Powerful hierarchy manipulation
- A coherency checking framework that ensures the correctness of the integrated design
- A generation framework that auto-creates a wide range of outputs including RTL, IP-XACT, verification and documentation views
- Fully customizable, template-based generators
- Rules specification IDE
- High performance, professional & scalable Eclipse-based tool
- Runs natively on Windows & Linux platforms

**Socrates Explorer**

**Hierarchy View**

**Problem Log**

**Integration Progress**



**Rules Specification**

**Progress Graph**

**Synthesis Summary**

## BENEFITS

### QUALITY

- Misinterpretation & misalignment bugs eliminated
- Auto-generation of consistent formats
- Correct-by-construction methodology

### SCHEDULE

- Fewer bugs reduces costly debug cycles
- Rapid turnaround time for incremental changes
- More predicability of project schedule

### PRODUCTIVITY

- Enhanced inter-team communications
- Fewer bugs means teams are more productive
- Automation replaces manual tasks

### PROFITABILITY

- Fewer resources through enhanced productivity
- Shorter, more predictable schedules reduce TTM
- Higher quality lowers risk of re-spin or TTM delays



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### About Duolog Technologies

Duolog Technologies is an award-winning provider of EDA tools and services that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates Chip Integration Hub employs a modular and extensible suite of tools for I/O layer definition, IP packaging, automated system assembly and register management.