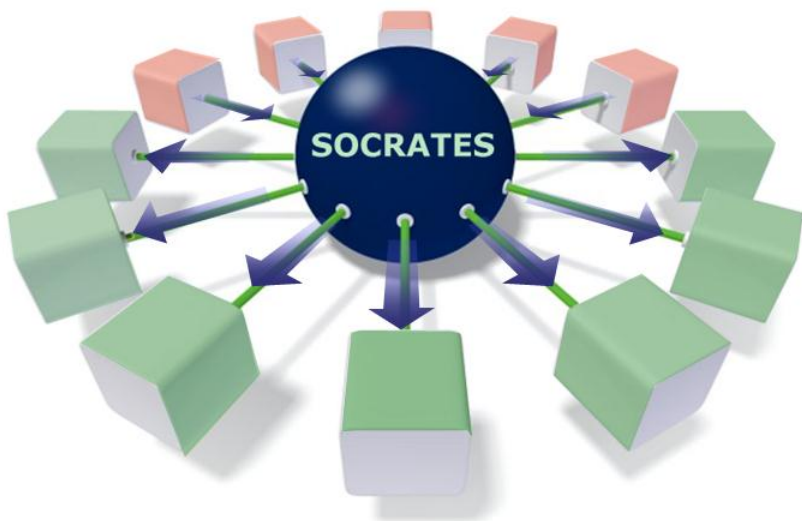


I/O Fabric Management



STANDARDIZE, CENTRALIZE, SYNCHRONIZE

The award-winning **Socrates Spinner** tool manages the complete specification of the I/O layer of a complex SoC, providing a fully automated, correct-by-construction methodology for creating the I/O fabric.

Spinner provides a single-source, standardized specification from which engineering teams draw the views that they require, ensuring that all teams are synchronized at all times.

Spinner auto-generates multiple views of the I/O fabric, including RTL, documentation and verification views, for use by design, verification, integration and back-end teams. The Spinner generators are fully customizable and new generators are quick and easy to create.

Spinner slashes workload and has been proven to deliver greater than **20% reduction** in the overall chip integration schedule.

Efficient, effective and robust chip integration is an essential element of any successful SoC development.

Time-to-market and cost pressures are dictating ever higher levels of IP use and reuse. Engineering teams are growing in size and diversity, with software playing an increasingly prominent role. These teams require simultaneous access to different views of the same design data throughout the lifetime of the project. It is vital that all teams access their information from a single source to avoid catastrophic data duplication, misinterpretation or misalignment errors.

The **Socrates Chip Integration Platform** acts as a hub for chip integration, standardizing IP and system metadata, centralizing design information and synchronizing design teams by auto-generating multiple views from a single, verified source.



Best Overall New Product Trendsetter

"TI has been using Duolog's Integration tools since 2002 on our OMAP SoC developments. Spinner has fully automated the creation and management of the I/O layers and has greatly enhanced the quality and timeliness of our deliverables"

OMAP Program Manager, Texas Instruments

SOCRATES SPINNER

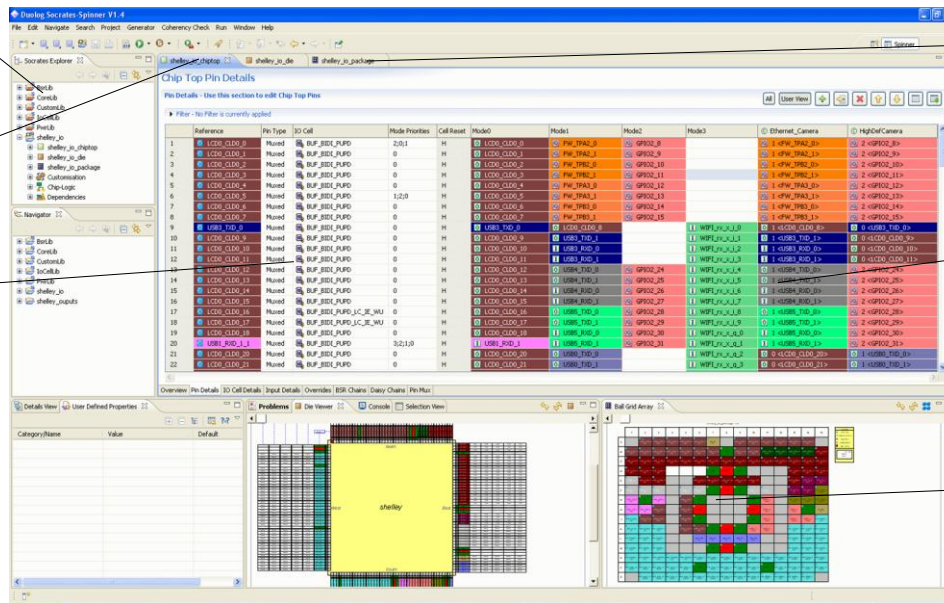
FEATURES

- Single-source repository for all I/O layer information
- Intuitive GUI and command-line interface for I/O specification capture, validation and generation
- Supports complex functional and test mux logic schemes, including logic equations
- Supports digital and analog I/O
- Automatic insertion of test and power isolation logic
- BGA, DIL and other common package types
- Import/export IP-XACT, Excel, HDL and other legacy formats
- Comprehensive DRC to ensure data coherency
- Multiple out-of-the-box generators including documentation, excel, I/O fabric RTL, TCL self-checking testbench, SystemVerilog and Specman verification infrastructures, JTAG BSDL
- Fully customizable, template-based generators

Specify I/O cells, Power cells, BSR cells

Capture all Pin details

Assign I/O cells



Capture die/package info

Handle pin muxing, DFT and I/O cell control

Integrate with physical design tools

BENEFITS

QUALITY

- Misinterpretation & misalignment bugs eliminated
- Auto-generation of consistent formats
- Correct-by-construction methodology

SCHEDULE

- Fewer bugs reduces costly debug cycles
- Rapid turnaround time for incremental changes
- More predicability of project schedule

PRODUCTIVITY

- Enhanced inter-team communications
- Fewer bugs means teams are more productive
- Automation replaces manual tasks

PROFITABILITY

- Fewer resources through enhanced productivity
- Shorter, more predictable schedules reduce TTM
- Higher quality lowers risk of re-spin or TTM delays



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About Duolog Technologies

Duolog Technologies is an award-winning provider of EDA tools and services that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates Chip Integration Hub employs a modular and extensible suite of tools for I/O layer definition, IP packaging, automated system assembly and register management.