

Efficient IP use/reuse is vital for cost-effective and predictable chip development. However, this IP-centric methodology is not without its challenges. Increasing complexity, parallel design flows, functionally & geographically diverse teams and multiple IP formats are putting immense pressure on product development. SOCRATES provides a solution for centralizing, standardizing and synchronizing IP data, creating a hub that ensures better design quality, better communications between design teams, more predictable schedules and, ultimately, lower cost development.

## Flow

### CAPTURE

Capture IP meta-data including interface, port and register information. Use IP-XACT or migrate legacy data from a range of different formats including documentation, excel, txt, and pdf. Enjoy quick and robust capture of hierarchical systems including HW/SW views



### VALIDATE

Run a wide range of DRC checks on all design data to ensure system coherency



### GENERATE

Generate source for architecture, hardware, software teams

- Generate IP and system-level views
- Generate design and verification views
- Generate design, implementation and review documentation



### COMMUNICATE

Propagate correct-by-construction views to implementation teams



## STANDARDIZE, CENTRALIZE, SYNCHRONIZE

SOCRATES enables quick and easy standardization and centralization of IP meta-data to create robust 'integration-ready' IP. This IP meta-data can be used as a source to generate a wide range of design implementation formats including documentation, RTL design code, HVL verification infrastructures and firmware libraries.

Socrates applications cover the full range of IP integration functions including:

- IP packaging and standardization
- Register and memory map management
- System assembly and interconnection
- Hierarchy manipulation/repartitioning
- I/O Integration

Socrates applications share IP data and allow full system integration from IP port to chip pin, as well as seamless HW/SW integration.

**Request a webinar today!**  
**Email : [webinar\\_request@duolog.com](mailto:webinar_request@duolog.com)**

## Benefits

### Better Communications

- Immediate documentation and implementation updates
- Auto-generation from single source
- No duplication of design data

### Better Design Quality

- Fewer bugs
- Consistent design collateral
- Correct-by-construction methodology
- Elimination of manual entry errors

### More Predictable Schedules

- Fastest integration flows
- Smoother HW/SW integration
- Fewer bugs = less debug
- Extensive IP and integration reuse
- Synchronized teams

### Reduced Costs

- Fewer resources through;
  - Higher levels of automation
  - Higher level of design reuse
  - Fewer bug fix cycles
- Less TTM/re-spin risk

*"[Socrates] is the centre-point of our design information and is used throughout the engineering functions in the company."*  
 SVP Product Development,  
 Intune Networks

*"Socrates ... has fully automated the creation and management of the I/O layers ... has greatly enhanced the quality and timeliness of our deliverables."*  
 Program Manager,  
 Texas Instruments

*"The integration of our NoC generation system with Duolog's viewing and validation capabilities provides a robust and efficient way to integrate complex SoCs."*  
 CEO,  
 Arteris

### About Duolog Technologies

Duolog Technologies is an award-winning provider of EDA tools and services that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates Chip Integration Hub employs a modular and extensible suite of tools for I/O layer definition, IP packaging, automated system assembly and register management.