

# SDRAM Verification IP

## Synthesizable Bus Functional Model

### Micron MT48LC4M32/16/8-B2

#### Features

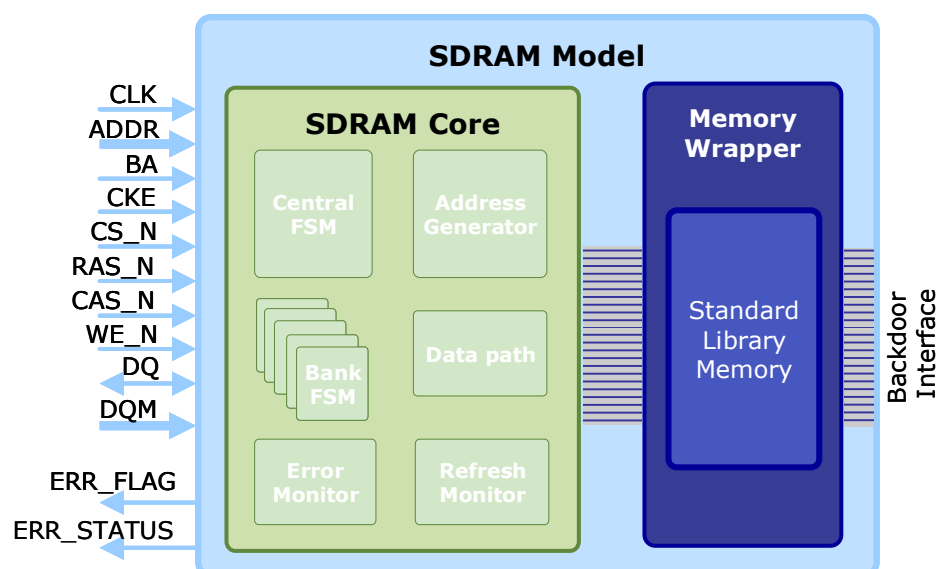
- Fully cycle accurate model
- Full command interpreter
- SDRAM-like RTL architecture
- Supports 32/16/8 Data Widths
- Accepts Single and Burst Accesses
- Implements Address Interleaving
- Supports 1-2-3 CAS Latency
- Full Mode Register access
- Use of Reserve bits to aid debug
- Access to user defined memory
- Supports concurrent auto-precharge
- Full Command Sequence monitoring
- Independent Bank state verification
- Auto/Self refresh monitoring
- Error Flag and Status for simple error monitoring
- Software access to error status and debug information
- Buffer stores command sequence for emulation debugging
- Command Time Stamps
- Targeted for FPGA Based systems (Xilinx/Altera) and ARM integrator
- Targeted for emulation systems (Palladium, V-Station)

#### Benefits

- Fully functional model for both simulation and emulation environment
- Full VHDL RTL available
- Works with Duolog's synthesizable modular testbenches
- Easy to use (includes user guide)
- Debugging capability

#### OVERVIEW

The synthesizable SDRAM model is a fully functional, cycle-accurate SDRAM model based on the Micron MT48LC4M32B2 that can be targeted to a range of emulation systems. The synthesizable SDRAM model enables the user to extensively debug their device in simulation and then conduct intensive validation in the emulation environment.



### Description

The MT48LC4M32 is a command based SDRAM with complex sequence based functionality including Read/Write bursts, initialisation and power down sequences, and pre-charge and refresh dependencies. This functionality is mirrored in this SDRAM model by the SDRAM core.

The core contains a Central FSM which interprets commands from the SDRAM interface and parses command sequences used for initialisation and high-level functions such as refresh, power down, etc. It stores the mode register and communicates with the Address Generator to handle bank addresses, interleaving, etc. It also communicates with the BANK FSMs for full data pipelining. The BANK

FSMs independently verify command sequences to ensure valid bank accesses.

The SDRAM core also contains a refresh monitor which ensures the correct timing of auto and self refreshes. Any errors that occur are flagged. These errors can be accessed by setting reserved bits in the mode register and standard SDRAM read accesses.

For further debug, a trace buffer can be accessed to allow interactive debug both in a simulation and emulation platform.

This model works out of the box within a wide range of emulation environments from custom emulation (Xilinx/Altera) systems to industry standard emulators.

### A Proven Track Record

Synthesizable BFM technology developed by Duolog has been proven and used extensively on more than 20 large scale System-on-Chip verification environments. The programming ease, test portability, and reusability of the technology across the various levels of hardware verification have all contributed to the success of our customers. Over 100 BFM's have been developed by Duolog.

### Evaluations

All of Duolog's synthesizable BFM's are available for evaluation. Contact us at [info@duolog.com](mailto:info@duolog.com) to obtain an evaluation copy or to request more information.

### About Duolog

Founded in 1999, Duolog Technologies is a supplier of market leading EDA tools and solutions enabling SoC Flow Automation.

Our tool offering is built on Socrates, a framework which enables rapid and effective SoC integration and verification of complex designs.

Tools within Socrates include SoC Register Management, Spirit-compliant SoC Connectivity, and Testbench Automation.

### Other Available Verification IP

⇒ Synthesizable memory models:

- SDRAM BFM (VHDL)
- NAND Flash BFM (VHDL)
- DDR2 BFM (VHDL)
- Mobile DDR BFM (VHDL)
- UtRAM BFM (Verilog)
- PSRAM BFM (Verilog)

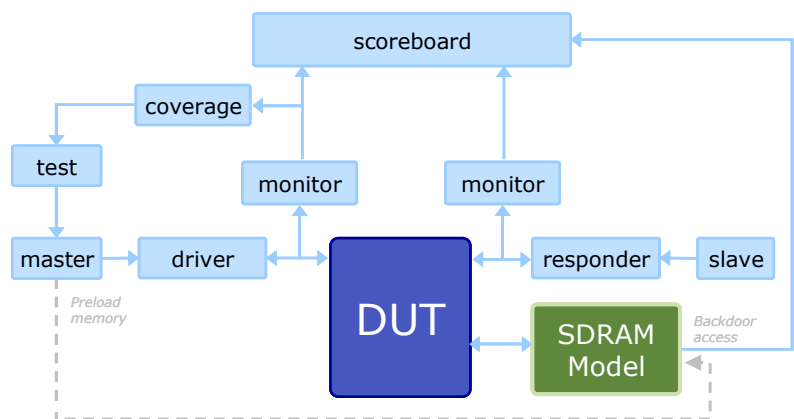
⇒ Transactional, synthesizable BFM technology:

- Helix™ microcontroller BFM framework (VHDL or Verilog)
- P1500 BFM (SystemVerilog & VHDL)
- UART BFM (VHDL)
- SPI BFM (VHDL)

⇒ 802.11 wireless models:

- 802.11abg MAC model (SystemC)
- 802.11abg PHY models (SystemC)
- RF channel model (SystemC)
- AHB and PCI drivers (SystemC)

### Module Validation



### System Validation

