

NAND FLASH Verification IP

Synthesizable Bus Functional Model

Samsung K9F2GXXX0M / Toshiba TC58NVG0S3AFT05

Features

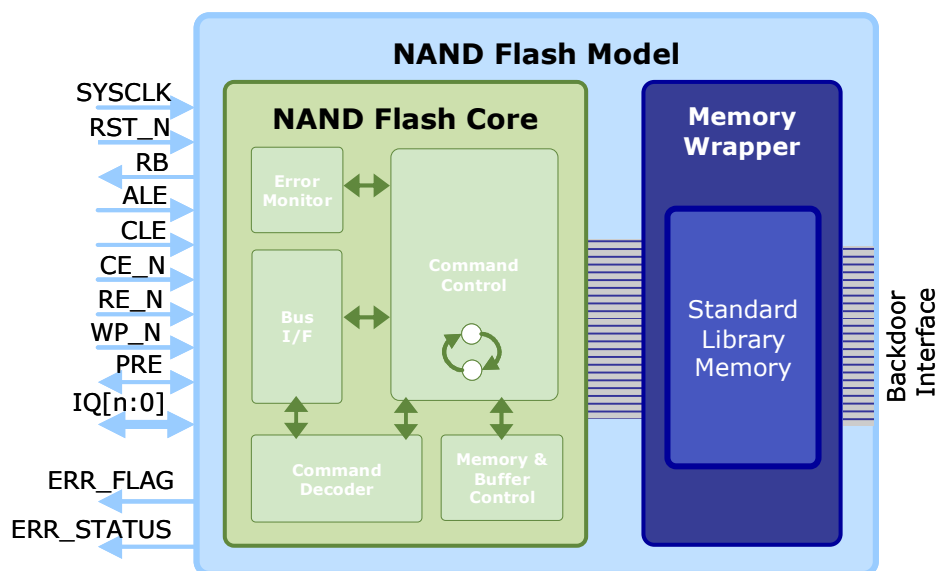
- Based on the latest Samsung and Toshiba NAND Flash devices
- Configurable as 1Gb, 2Gb, 4Gb, or 8Gb+
- Full NAND Flash command set
- Supports x8 and x16 configurations
- Configurable timings for Program/Erase/Read operations
- Configurable Block and Page size
- Configurable Main/Spare area size
- Supports 4, 5, or 6 cycle addressing
- Supports Cache Program
- Supports Copy-Back Program
- Supports Random Data Input/Output
- Supports Power-On Auto Read
- Supports 'Chip Enable Don't Care'
- Fully synthesizable code
- Full validation coverage
- Access to user defined memory
- User configurable scratch memory size
- Full Command Sequence monitoring
- Accurate Program/Erase/Read latency emulation
- Read/Write Pulse Width Monitor
- Error Flag and Status for simple error monitoring
- Backdoor memory interface
- Targeted for FPGA based systems (Xilinx/Altera) and ARM integrator
- Targeted for emulation systems (Palladium, V-Station)

Benefits

- Fully functional model for both simulation and emulation environment
- Full VHDL RTL available
- Works with Duolog's synthesizable modular testbenches
- Easy to use (includes user guide)
- Debugging capability

OVERVIEW

The synthesizable NAND Flash model is a fully functional and configurable model based on the latest Samsung and Toshiba devices that can be targeted to a range of emulation systems. The synthesizable NAND Flash enables the user to extensively debug their device in simulation and then conduct intensive validation in the emulation environment.



Product Brief

Description

The Samsung and Toshiba NAND Flash devices are command-based Electrically Erasable and Programmable Read-Only Memories with a multiplexed command/address bus. The devices allow both serial page read/program and random column data accesses. This functionality is mirrored in the NAND Flash model by the NAND Flash core.

The core contains a command decoder which interprets commands from the NAND Flash interface and parses command sequences to a central FSM. The FSM communicates with the Memory and Buffer Control to perform the memory accesses. The FSM verifies command

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sequences and addresses to ensure valid accesses and emulates the required latencies for Program/Erase/Read operations.

The NAND Flash core contains timing monitors which verify minimum read/write pulse widths and minimum spacing between successive cycles. Any errors that occur are flagged and the cause of the error is indicated on the error status bus.

This model works out of the box within a wide range of emulation environments from custom emulation (Xilinx/Altera) systems to industry standard emulators.

A Proven Track Record

Synthesizable BFM technology developed by Duolog has been proven and used extensively on more than 20 large scale System-on-Chip verification environments. The programming ease, test portability, and reusability of the technology across the various levels of hardware verification have all contributed to the success of our customers. Over 100 BFM have been developed by Duolog.

Evaluations

All of Duolog's synthesizable BFM are available for evaluation. Contact us at info@duolog.com to obtain an evaluation copy or to request more information.

About Duolog

Founded in 1999, Duolog Technologies is a supplier of market leading EDA tools and solutions enabling SoC Flow Automation.

Our tool offering is built on Socrates, a framework which enables rapid and effective SoC integration and verification of complex designs.

Tools within Socrates include SoC Register Management, Spirit-compliant SoC Connectivity, and Testbench Automation.

Other Available Verification IP

⇒ Synthesizable memory models:

- SDRAM BFM (VHDL)
- NAND Flash BFM (VHDL)
- DDR2 BFM (VHDL)
- Mobile DDR BFM (VHDL)
- UtRAM BFM (Verilog)
- PSRAM BFM (Verilog)

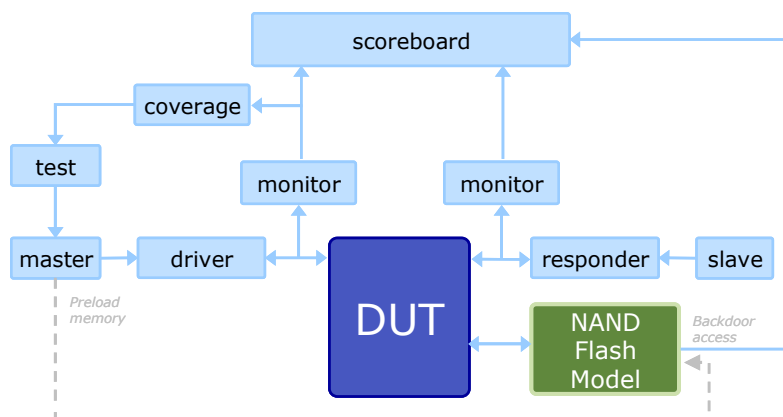
⇒ Transactional, synthesizable BFM technology:

- Helix™ microcontroller BFM framework (VHDL or Verilog)
- P1500 BFM (SystemVerilog & VHDL)
- UART BFM (VHDL)
- SPI BFM (VHDL)

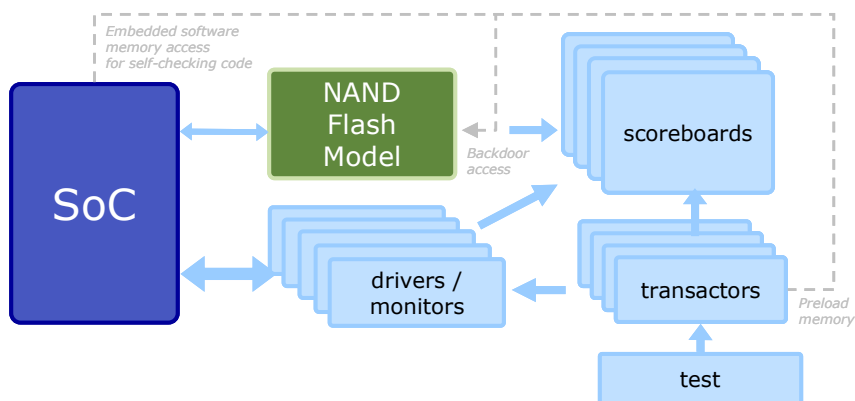
⇒ 802.11 wireless models:

- 802.11abg MAC model (SystemC)
- 802.11abg PHY models (SystemC)
- RF channel model (SystemC)
- AHB and PCI drivers (SystemC)

Module Validation



System Validation



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