

# Mobile DDR SDRAM Verification IP

## Synthesizable Bus Functional Model

### Micron MT46H Series

**Features**

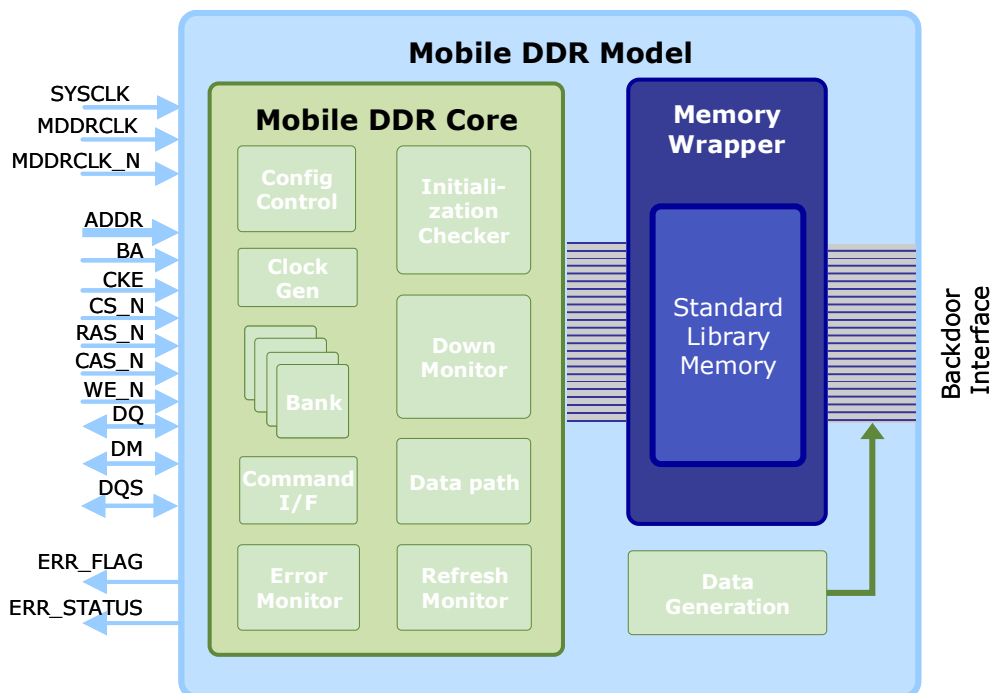
- Fully cycle accurate model
- Full command interpreter
- Configurable as 256Mb, 512Mb, or 1Gb
- Supports 32 or 16 bit Data Widths
- Four Bank configurations
- Burst Lengths of 2, 4, 8 and 16, and Continuous Page
- Supports Sequential & Address Interleaving
- Supports 2-3 CAS Latency
- Full Mode Registers access
- Use of Reserve bits to aid debug
- Access to user defined memory
- Supports concurrent reads and writes with auto-precharge
- Data corruption generation for deep-power down and self-refresh modes
- Full Initialization and Command Sequence monitoring
- Power Down Entry/Exit Monitor
- Independent Bank state verification
- Auto/Self refresh monitoring
- Error Flag / Status for simple error monitoring
- Software access to error status and debug information
- Buffer stores command sequence for emulation debugging
- Command Time Stamps
- Targeted for FPGA Based systems (Xilinx/Altera) and ARM integrator
- Targeted for emulation systems (Palladium, V-Station)

**Benefits**

- Fully functional model for both simulation and emulation environment
- Full VHDL RTL available
- Works with Duolog's synthesizable modular testbenches
- Easy to use (includes user guide)
- Debugging capability

**OVERVIEW**

The synthesizable Mobile DDR model is a fully functional, configurable, and cycle-accurate Mobile DDR model based on the Micron MT46H series that can be targeted to a range of emulation systems. The synthesizable Mobile DDR model enables the user to extensively debug their device in simulation and then conduct intensive validation in the emulation environment.



**Description**

The MT46H series are command based Mobile DDR modules with complex sequence based functionality including Read/Write bursts, initialization, power down sequences, pre-charge, and refresh dependencies. This model exceeds the JESD79-2A standard DDR SDRAM and provides the Mobile DDR behaviour.

The core contains a Central FSM which interprets commands from the Mobile DDR interface and parses command sequences used for initialization and high-level functions such as refresh, power down, etc. It stores the mode register and communicates with the Address Generator to handle bank addresses, interleaving, etc. It also communicates with the BANK FSMs for full data pipelining. The BANK

FSMs independently verify command sequences to ensure valid bank accesses.

The Mobile DDR core also contains a refresh monitor which ensures the correct timing of auto and self refreshes. Any errors that occur are flagged. These errors can be accessed by setting reserved bits in the mode register and standard Mobile DDR read accesses.

For further debug, a trace buffer can be accessed to allow interactive debug both in a simulation and emulation platform.

This model works out of the box within a wide range of emulation environments from custom emulation (Xilinx/Altera) systems to industry standard emulators.

**A Proven Track Record**

Synthesizable BFM technology developed by Duolog has been proven and used extensively on more than 20 large scale System-on-Chip verification environments. The programming ease, test portability, and reusability of the technology across the various levels of hardware verification have all contributed to the success of our customers. Over 100 BFM's have been developed by Duolog.

**Evaluations**

All of Duolog's synthesizable BFM's are available for evaluation. Contact us at [info@duolog.com](mailto:info@duolog.com) to obtain an evaluation copy or to request more information.

**About Duolog**

Founded in 1999, Duolog Technologies is a supplier of market leading EDA tools and solutions enabling SoC Flow Automation.

Our tool offering is built on Socrates, a framework which enables rapid and effective SoC integration and verification of complex designs.

Tools within Socrates include SoC Register Management, Spirit-compliant SoC Connectivity, and Testbench Automation.

**Other Available Verification IP**

⇒ Synthesizable memory models:

- SDRAM BFM (VHDL)
- NAND Flash BFM (VHDL)
- DDR2 BFM (VHDL)
- Mobile DDR BFM (VHDL)
- UtRAM BFM (Verilog)
- PSRAM BFM (Verilog)

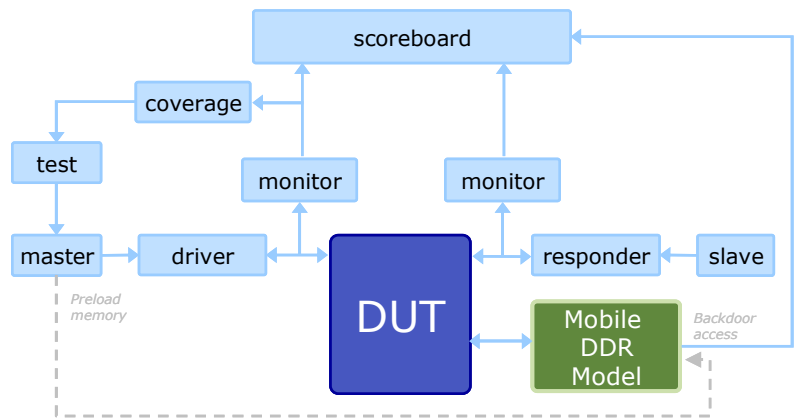
⇒ Transactional, synthesizable BFM technology:

- Helix™ microcontroller BFM framework (VHDL or Verilog)
- P1500 BFM (SystemVerilog & VHDL)
- UART BFM (VHDL)
- SPI BFM (VHDL)

⇒ 802.11 wireless models:

- 802.11abg MAC model (SystemC)
- 802.11abg PHY models (SystemC)
- RF channel model (SystemC)
- AHB and PCI drivers (SystemC)

Module Validation



System Validation

