

DDR3 SDRAM Verification IP

Synthesizable Bus Functional Model

Based on JEDEC JESD79-3 DDR3 standard

Features

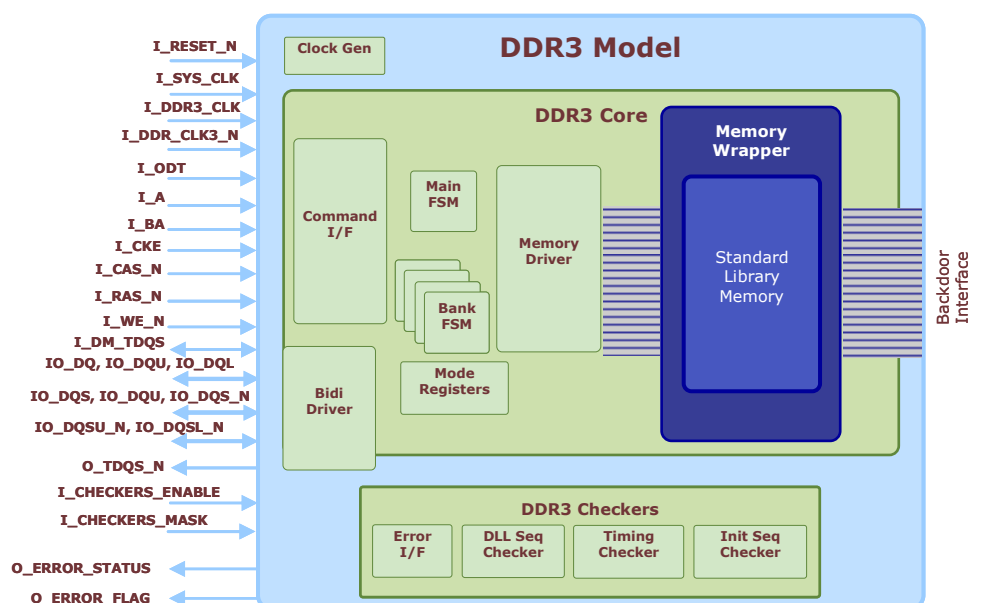
- Fully cycle accurate model
- Full command interpreter
- Flexible configuration sizes
- Supports 4, 8 or 16 bit Data Widths
- 8 Bank configuration
- Burst Lengths of 4, 8 and 16, and Continuous Page
- Supports Read Latency from 2 - 8
- Full Mode Registers access
- Back Door memory interface
- Supports concurrent reads and writes with auto-precharge
- Full Initialization and Command Sequence monitoring
- Power Down Entry/Exit Monitor
- Independent Bank state verification
- Auto/Self refresh monitoring
- Error Flag / Status for simple error monitoring
- Targeted for FPGA Based systems (Xilinx/Altera) and ARM integrator
- Targeted for emulation systems (Palladium, V-Station)

Benefits

- Fully functional model for both simulation and emulation environment
- Full VHDL RTL available
- Easy to use (includes detailed user guide)
- Debugging capability
- Wide Range of protocol and timing checks

OVERVIEW

The Duolog synthesizable DDR3 model is a fully functional, configurable, and cycle-accurate model based on the JEDEC ESD79-3 DDR3 standard that can be targeted to a range of emulation systems. The synthesizable DDR3 model enables the user to extensively debug their device in simulation and then conduct intensive validation in the emulation environment.



Description

The DDR3 SDRAM is a command based module with complex sequence based functionality including Read/Write bursts, initialization, power down sequences, pre-charge, and refresh dependencies. This model provides the DDR3 behaviour.

The core contains a data interface Central FSM which interprets and synchronizes commands from the DDR3 interface and parses command sequences used for initialization and high-level functions such as refresh, power down, etc. It stores the mode register and communicates with the Address Generator to handle bank addresses, interleaving, etc. The BANK FSMs independently verify command sequences to ensure valid bank accesses.

The DDR3 core also contains a refresh monitor which ensures the correct timing of auto and self refreshes. Any errors that occur are flagged. The DDR3 BFM allows the user the ability to disable the displaying of errors for logical error groups independently.

This model works out of the box within a wide range of emulation environments from custom emulation (Xilinx/Altera) systems to industry standard emulators.

A Proven Track Record

Synthesizable BFM technology developed by Duolog has been proven and used extensively on more than 20 large scale System-on-Chip verification environments. The programming ease, test portability, and reusability of the technology across the various levels of hardware verification have all contributed to the success of our customers. Over 100 BFMs have been developed by Duolog.

Evaluations

All of Duolog's synthesizable BFMs are available for evaluation. Contact us at info@duolog.com to obtain an evaluation copy or to request more information.

About Duolog

Founded in 1999, Duolog Technologies is a supplier of market leading EDA tools and solutions enabling SoC Flow Automation.

Our tool offering is built on Socrates, a framework which enables rapid and effective SoC integration and verification of complex designs.

Tools within Socrates include SoC Register Management, Spirit-compliant SoC Connectivity, and Testbench Automation.

Other Available Verification IP

⇒ Synthesizable memory models:

- LPDDR2 BFM (VHDL)
- SDRAM BFM (VHDL)
- NAND Flash BFM (VHDL)
- DDR2 BFM (VHDL)
- Mobile DDR BFM (VHDL)

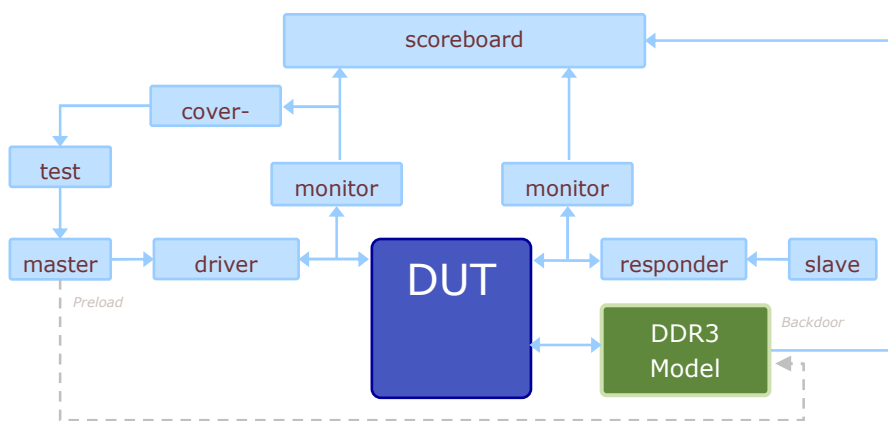
⇒ Transactional, synthesizable BFM technology:

- Helix™ microcontroller BFM framework (VHDL or Verilog)
- P1500 BFM (SystemVerilog & VHDL)
- UART BFM (VHDL)
- SPI BFM (VHDL)

⇒ 802.11 wireless models:

- 802.11abg MAC model (SystemC)
- 802.11abg PHY models (SystemC)
- RF channel model (SystemC)
- AHB and PCI drivers (SystemC)

Module Validation



System Validation

