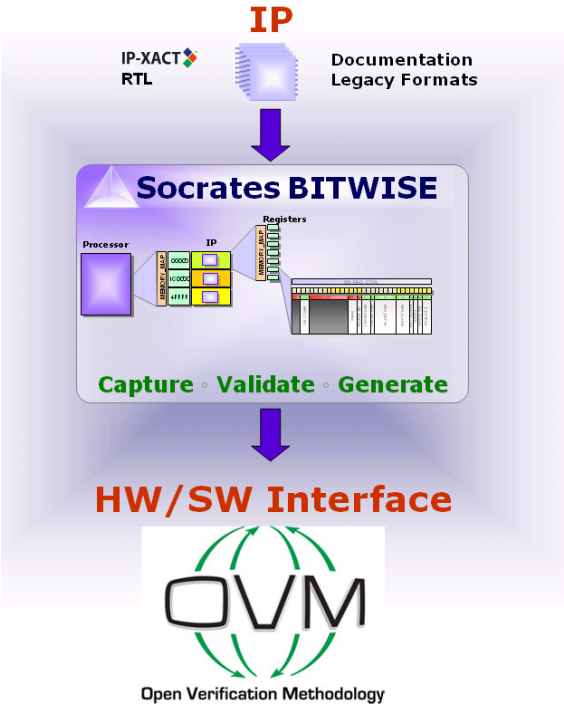
OVM SystemVerilog Generator

Duolog Technologies

Auto-generate SystemVerilog code for OVM-based verification flows using the **Bitwise** Register Management tool from Duolog

Open Verification Methodology (OVM) generators from Duolog create the register and memory map package information for your system components from a single source register specification. The OVM_SV generator output includes specific extensions from the Mentor Graphics OVM register package to allow for seamless integration with OVM 2.0/2.0.1 compatible tools that support the Mentor packages and flows.



OVM_SV Features

- Auto-generates complete OVM Register file (.sv) class descriptions, including:
  - ⇒ Register Structure definitions
  - ⇒ typedef structures detailing bitfield names, widths etc.
  - ⇒ Power on reset values
  - ⇒ Data masks for Register Read/Write accesses
- Uses Mentor OVM 1.0-Beta6/7 register package extensions
- Compatible with OVM 2.0 tools and Mentor's Questa Verification Platform
- Enables an IP-XACT to OVM Flow
- Fully customisable output format

The Bitwise OVM generator creates complete SystemVerilog register descriptions for IP components. In addition to a fully interactive capture GUI, Bitwise supports IP-XACT import allowing for a complete **IP-XACT to OVM flow**.

The auto-generated SystemVerilog (.sv) files contain a full description of memory-mapped registers, including name, width, reset, read masks, write masks. The files operate with the standard OVM packages and use constructs described by the Mentor OVM register package extensions. They can be used with any OVM 2.0 or 2.0.1 compatible tools - including Mentor's Questa Verification Platform.

Because the OVM models are generated from a central source, they are guaranteed to be consistent with other Bitwise generated views such as documentation, C API, VR_AD, VHDL/Verilog etc.

About Bitwise:

Bitwise provides a single-source definition for all register and memory map information associated with an IP, Subsystem or SoC. It allows all stakeholders to see a coherent, in-sync, up-to-date picture of the status of the design. All information, whether captured, imported or linked can be elaborated and rendered ensuring robust data coherency at all times. Fully customizable generator templates provide a powerful and user-friendly way to modify or create generators.

Need more information? See **www.duolog.com** or contact **sales@duolog.com**

About Duolog

Founded in 1999, Duolog Technologies is a supplier of market leading EDA tools focused on streamlining SoC Integration. Our tool offerings include Socrates, a suite of integration tools which enable rapid and effective SoC integration and verification of complex designs. This suite of tools include SoC Register Management, IO Fabric Generation, SoC assembly, testbench automation and bus transaction analysis tools. Complementary to our EDA offerings Duolog also provide leading edge IC integration, design and verification services.