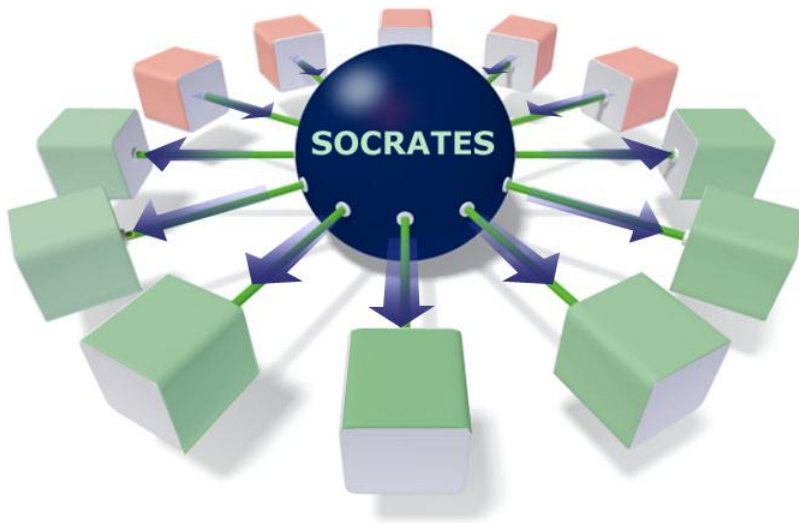


Managing the HW/SW Interface



STANDARDIZE, CENTRALIZE, SYNCHRONIZE

Socrates Bitwise manages the complete register and memory infrastructure for an IP, sub-system or SoC. Bitwise provides a single-source specification from which engineering teams draw the views that they require, ensuring that all teams are synchronized at all times.

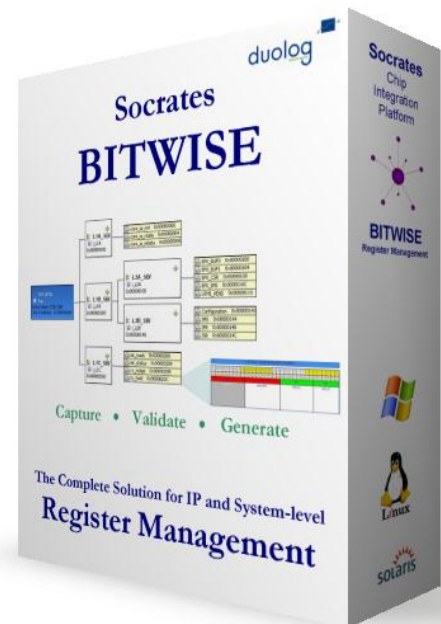
Bitwise generators auto-create code and documentation for design, verification, software and integration teams. Bitwise generators are fully customizable and new generators are quick and easy to create.

Bitwise slashes workload, promotes inter-team communication and improves overall design quality. Bitwise is the only commercial register and memory management tool with over 70 tape-outs to its credit.

Efficient, effective and robust chip integration is an essential element of any successful SoC development.

Time-to-market and cost pressures are dictating ever higher levels of IP use and reuse. Engineering teams are growing in size and diversity, with software playing an increasingly prominent role. These teams require simultaneous access to different views of the same design data throughout the lifetime of the project. It is vital that all teams access their information from a single source to avoid catastrophic data duplication, misinterpretation or misalignment errors.

The **Socrates Chip Integration Platform** acts as a hub for chip integration, standardizing IP and system metadata, centralizing design information and synchronizing design teams by auto-generating multiple views from a single, verified source.

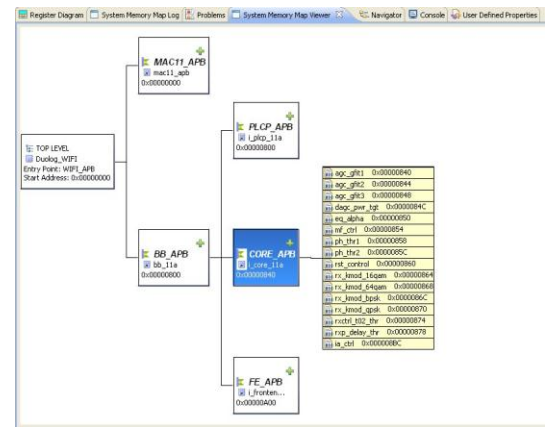
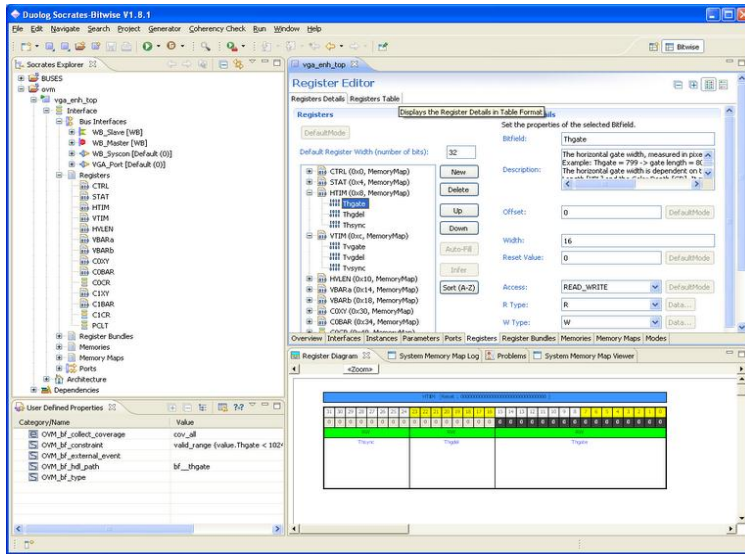


"Bitwise has enhanced the productivity of our design flow, making our development process more efficient and less labour intensive... [Bitwise] is the centre-point of this design information and is used throughout the engineering functions in the company"

SVP, Product Development, Intune Networks

FEATURES

- Single-source repository for all register and memory-map data
- Full-scope IP packaging including ports & interfaces
- Supports hierarchical systems & memory-maps
- Import/export IP-XACT, Excel and other legacy formats
- Advanced register/bitfield configurations
- Configurable & extensible register access types
- Data-model extension via user-defined properties
- Comprehensive DRC to ensure data coherency
- Multiple out-of-the-box generators including documentation, TLM, RTL, verification and software views
- Fully customizable, template-based generators
- High performance, professional & scalable Eclipse-based tool
- Runs natively on Windows & Linux platforms



BENEFITS

QUALITY

- Misinterpretation & misalignment bugs eliminated
- Auto-generation of consistent formats
- Correct-by-construction methodology

SCHEDULE

- Fewer bugs reduces costly debug cycles
- Rapid turnaround time for incremental changes
- More predicability of project schedule

PRODUCTIVITY

- Enhanced inter-team communications
- Fewer bugs means teams are more productive
- Automation replaces manual tasks

PROFITABILITY

- Fewer resources through enhanced productivity
- Shorter, more predictable schedules reduce TTM
- Higher quality lowers risk of re-spin or TTM delays



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About Duolog Technologies

Duolog Technologies is an award-winning provider of EDA tools and services that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates Chip Integration Hub employs a modular and extensible suite of tools for I/O layer definition, IP packaging, automated system assembly and register management.